

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1859	mtj	US-PGPUB; USPAT	OR	ON	2006/06/06 15:36
L2	7006	perpendicular adj magnet\$	US-PGPUB; USPAT	OR	ON	2006/06/06 15:37
L3	153	1 and 2	US-PGPUB; USPAT	OR	ON	2006/06/06 15:37
L4	373588	diode	US-PGPUB; USPAT	OR	ON	2006/06/06 15:37
L5	33	3 and 4	US-PGPUB; USPAT	OR	ON	2006/06/06 15:37
L6	549	1 and 4	US-PGPUB; USPAT	OR	ON	2006/06/06 15:37
L7	1478	365/158.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/06 15:37
L8	1378	365/171.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/06 15:37
L9	914	365/173.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/06 15:38
L10	176	1 and 4 and 7	US-PGPUB; USPAT	OR	ON	2006/06/06 15:38
L11	139	1 and 4 and 8	US-PGPUB; USPAT	OR	ON	2006/06/06 15:38
L12	108	1 and 4 and 9	US-PGPUB; USPAT	OR	ON	2006/06/06 15:38
L13	8	ho-chiahua.in.	US-PGPUB; USPAT	OR	ON	2006/06/06 15:38

PALM INTRANET

Day : Tuesday
 Date: 6/6/2006
 Time: 15:39:44

Inventor Name Search Result

Your Search was:

Last Name = HO

First Name = CHIAHUA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>10437852</u>	7020009	150	05/14/2003	BISTABLE MAGNETIC DEVICE USING SOFT MAGNETIC INTERMEDIARY MATERIAL	HO, CHIAHUA
<u>10715670</u>	Not Issued	71	11/17/2003	Perpendicular MRAM with high magnetic transition and low programming current	HO, CHIAHUA
<u>10735114</u>	Not Issued	71	12/12/2003	Method and apparatus for a low write current MRAM having a write magnet	HO, CHIAHUA
<u>10791911</u>	Not Issued	71	03/03/2004	MRAM array employing spin-filtering element connected by spin-hold element to MRAM cell structure for enhanced magnetoresistance	HO, CHIAHUA
<u>10904477</u>	Not Issued	41	11/12/2004	HIGH-SELECTIVITY ETCHING PROCESS	HO, CHIAHUA
<u>10907442</u>	7053406	150	04/01/2005	ONE-TIME PROGRAMMABLE READ ONLY MEMORY AND MANUFACTURING METHOD THEREOF	HO, CHIAHUA
<u>11197659</u>	Not Issued	20	08/04/2005	Non-volatile memory cells and methods of manufacturing the same	HO, CHIAHUA
<u>11203087</u>	Not Issued	30	08/15/2005	Method of manufacturing a non-volatile memory device	HO, CHIAHUA
<u>11223548</u>	Not Issued	41	09/09/2005	Bistable magnetic device using soft magnetic intermediary material	HO, CHIAHUA
<u>11234983</u>	Not Issued	30	09/26/2005	Dual gate multi-bit semiconductor memory	HO, CHIAHUA
<u>11255606</u>	Not Issued	30	10/21/2005	Magnetic memory device and methods for making a magnetic memory device	HO, CHIAHUA

<u>11279945</u>	Not Issued	20	04/17/2006	Memory device and manufacturing method	HO, CHIAHUA
<u>11281018</u>	Not Issued	30	11/17/2005	Systems and methods for a magnetic memory device that includes two word line transistors	HO, CHIAHUA
<u>11281027</u>	Not Issued	30	11/17/2005	Systems and methods for a magnetic memory device that includes a single word line transistor	HO, CHIAHUA
<u>11281658</u>	Not Issued	30	11/17/2005	Systems and methods for reading and writing a magnetic memory device	HO, CHIAHUA
<u>11332748</u>	Not Issued	30	01/13/2006	Structure and method for a magnetic memory device with proximity writing	HO, CHIAHUA
<u>11352788</u>	Not Issued	30	02/13/2006	Dual-gate, non-volatile memory cells, arrays thereof, methods of manufacturing the same and methods of operating the same	HO, CHIAHUA
<u>11356659</u>	Not Issued	20	02/17/2006	Dual gate multi-bit semiconductor memory array	HO, CHIAHUA
<u>11357902</u>	Not Issued	30	02/17/2006	Memory cell device and manufacturing method	HO, CHIAHUA
<u>11360447</u>	Not Issued	20	02/23/2006	Chalcogenide layer etching method	HO, CHIAHUA
<u>11381939</u>	Not Issued	25	05/05/2006	METHODS AND APPARATUS FOR THERMALLY ASSISTED PROGRAMMING OF A MAGNETIC MEMORY DEVICE	HO, CHIAHUA
<u>11381973</u>	Not Issued	20	05/05/2006	Structures and Methods of a Bistable Resistive Random Access Memory	HO, CHIAHUA
<u>11382422</u>	Not Issued	19	01/01/0001	Bridge Resistance Random Access Memory Device and Method With A Singular Contact Structure	HO, CHIAHUA
<u>11382799</u>	Not Issued	19	05/11/2006	Manufacturing Method for Phase Change RAM with Electrode Layer Process	HO, CHIAHUA
<u>11420930</u>	Not Issued	19	01/01/0001	MAGNETIC RANDOM ACCESS MEMORY USING SINGLE CRYSTAL SELF-ALIGNED DIODE	HO, CHIAHUA
<u>60738924</u>	Not Issued	20	11/22/2005	Memory cell device and manufacturing method	HO, CHIAHUA

<u>60739089</u>	Not Issued	20	11/21/2005	Air cell thermal isolation for a phase change memory array	HO, CHIAHUA
<u>60742448</u>	Not Issued	20	12/05/2005	Manufacturing method phase change ram with electrode layer process	HO, CHIAHUA
<u>60754161</u>	Not Issued	20	12/27/2005	Method for forming self-aligned thermal isolation cell for a phase change memory array	HO, CHIAHUA
<u>60757341</u>	Not Issued	20	01/09/2006	Method for fabricating a pillar-shaped phase change memory element	HO, CHIAHUA

Inventor Search Completed: No Records to Display.

Search Another: Inventor

Last Name	First Name
<input type="text" value="ho"/>	<input type="text" value="chiahua"/>
<input type="button" value="Search"/>	

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